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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LEFKOWITZ, SUMATI	

ART UNIT	PAPER NUMBER
2189	21

DATE MAILED: 11/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/668,952	HORDEN ET AL.	
	Examiner	Art Unit	
	Sumati Lefkowitz	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 38-61* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 38-61* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-13 and 38-61 are pending.

2. While all the claims have been examined in the interest of expediting prosecution of the application, Applicant is requested to correct the reissue application so that it is compliant with 37 CFR 1.173 c, d1, and d2.

Claim Rejections - 35 USC § 251

3. Claim 7, 12, 38, 41, 46, 49, 53, 56, and 59 rejected under 35 U.S.C. 251 as being an improper recapture of broadened claimed subject matter surrendered in the application for the patent upon which the present reissue is based. See *Hester Industries, Inc.* v. *Stein, Inc.*, 142 F.3d 1472, 46 USPQ2d 1641 (Fed. Cir. 1998); *In re Clement,* 131 F.3d 1464, 45 USPQ2d 1161 (Fed. Cir. 1997)*; Ball Corp.* v. *United States*, 729 F.2d 1429, 1436, 221 USPQ 289, 295 (Fed. Cir. 1984). A broadening aspect is present in the reissue which was not present in the application for patent. The record of the application for the patent shows that the broadening aspect (in the reissue) relates to subject matter that applicant previously surrendered during the prosecution of the application. Accordingly, the narrow scope of the claims in the patent was not an error within the meaning of 35 U.S.C. 251, and the broader scope surrendered in the application for the patent cannot be recaptured by the filing of the present reissue application.

Claims 7, 12, 38, 41, 46, 49, 53, 56, and 59 do not contain subject matter which was used to distinguish the originally filed claims from the prior art during the prosecution of the

application. Specifically, the claims do not contain any recitation of the following limitations, or equivalent substitutes/replacements for the following limitations:

- an operating system running on the processor, monitoring an application mix executing in the processor to determine a required frequency, determining a minimum voltage at which the processor core can operate at the required frequency, wherein the operating system directs the state machine to enter a state in which the required frequency is supplied by the clock signal generator and a closest supported voltage equal to or greater than the minimum voltage is supplied by the voltage regulator
- accepting a measure of processor core performance need of each application currently seeking access to the processor core, accumulating each measure of processor core performance need to find total current need, calculating a minimum frequency that will allow the processor core to meet the total current need for the time period, selecting the lowest supported frequency equal to or greater than the minimum frequency to be a required frequency
- reducing power consumption by a processor core and a pad ring comprising finding a minimum supported voltage at which the processor core can operate at the required frequency independent of a voltage required by the pad ring, supplying the required frequency and the minimum supported voltage to the processor core, and dynamically changing the required frequency and the minimum supported voltage supplied responsive to a change in the current application mix

In addition, the claims are broader even in scope than canceled claim 1 and originally filed claims 8, 14, and 16.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 4, 12, 13, 38-40, 49-52, and 59-61 are rejected under 35 U.S.C. 102(e) as being anticipated by Fung 2002/0007463 A1, with Fung 5,710,929 incorporated by reference.

a. As to claim 4, Fung discloses a method of reducing power consumption by a processor core comprising the steps of accepting a measure of processor core performance need of each application currently seeking access to the processor core, accumulating each measure of processor core performance need to find total current need (note Fung '929: column 8, line 13 – column 11, line 37), calculating a minimum frequency that will allow the processor core to meet

the total current need for the time period (note Fung '929: column 15, line 35 – column 16, line 62), selecting a lowest supported frequency equal to or greater than the minimum frequency to be a required frequency (note Fung '463: [0056], finding a minimum supported voltage at which the processor core can operate at the required frequency (note Fung '463: [0035, 0056, 0069, 0070, 0072]), supplying the required frequency and the minimum supported voltage to the processor core (note Fung '463: [0035, 0056, 0069, 0070, 0072]) and dynamically changing the required frequency and the minimum supported voltage supplied responsive to a change in the current application mix (note Fung '463: [0035, 0056, 0069, 0070, 0072, 0151]).

b. As to claims 12 and 13, Fung discloses a method comprising determining an instruction mix of a processor (note Fung '929: column 8, line 13 – column 11, line 16), determining a frequency at which the processor may operate given the instruction mix (note Fung '929: column 15, line 35 – column 16, line 62), and determining a voltage potential level corresponding to the frequency and providing at least a portion of a processor with the frequency and voltage potential level (note Fung '463: [0035, 0056, 0069, 0070, 0072, 0151]), further comprising changing the frequency and voltage potential in response to a change in the instruction mix of the processor (note Fung '463: [0035, 0056, 0069, 0070, 0072, 0151]).

c. As to claims 38-40, Fung discloses a method of operating a processor comprising monitoring an application mix executed by a processor (note Fung '929: column 8, line 13 – column 11, line 16), and adjusting the voltage potential level provided to at least a portion of the processor based on the application mix executed by the processor (note Fung '463: [0035, 0056, 0069, 0070, 0072, 0151]), further comprising determining an operational frequency based on the instruction mix executed by the processor (note Fung '929: column 15, line 35 – column 16, line

62), further comprising adjusting the operational frequency after adjusting the voltage potential level (note Fung '463: [0035, 0056, 0069, 0070, 0072, 0151]).

d. As to claims 49-52, Fung discloses an apparatus comprising a processor (note Fung '463: Figure 2, element 320), a voltage regulator (note Fung '463: Figure 2, element 324) adapted to provide at least two voltage potential levels to at least a portion of the processor, and wherein the voltage potential level provided by the voltage regulator is adapted to be adjusted depending on the operational load of the processor and is provided to an electrically common terminal in the processor (note Fung '463: [0035, 0056, 0069, 0070, 0072, 0151]), wherein the voltage regulator is further adapted to provide the voltage potential level depending on an operational frequency of the processor (note Fung '463: [0035, 0056, 0069, 0070, 0072, 0151]), further comprising a state machine responsive to an operational load of the processor (note Fung '929: state control unit 23 of column 6, lines 15-39), wherein the processor is adapted to receive a clock signal that is varied in accordance with changes in the operational load of the processor (note Fung '463: [0035, 0056, 0069, 0070, 0072, 0151]).

e. As to claims 59-61, Fung discloses an apparatus comprising a state machine (note Fung '929: state control unit 23 of column 6, lines 28-35) adapted to determine a frequency for an application mix (note Fung '929: column 8, line 13 – column 11, line 16), wherein the state machine is further adapted to provide a voltage potential to at least a core of a processor for the frequency (note Fung '463: [0035, 0056, 0069, 0070, 0072]), further comprising a voltage regulator (note Fung '463: Figure 2, element 324) to provide the voltage potential level, wherein the processor is adapted to receive a clock signal that is varied in accordance with changes in the application mix of the processor (note Fung '929: column 8, line 13 – column 11, line 16).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 1-3, 5, 6, and 56-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fung 2002/0007463 A1, with Fung 5,710,929 incorporated by reference, in view of Applicant's Admitted Prior Art (hereinafter AAPA).

a. As to claims 1-3, 5, 6, and 56-58, Fung discloses a system comprising a processor (note Fung '463: Figure 2, element 320) coupled to a memory (note Fung '463: Figure 2, elements 328, 338) by a bus (note Fung '463: Figure 2, element 336, 329, 339), the processor having a processor core, the processor core having a power supply (i.e., inherent), a voltage regulator (note Fung '463: Figure 2, element 324) providing a plurality of voltages and providing

the power supply, a clock signal generator (note Fung '463: Figure 2, element 342) providing a clock signal at a plurality of frequencies, a state machine (note Fung '929: state control unit 23 of column 6, lines 15-39) to coordinate voltage and clock frequency to the processor core (note Fung '929: column 6, lines 28-35), and an operating system running on the processor (note Fung '929: column 2, lines 49-53, column 3, lines 1-10, column 5, lines 55-59, column 10, line 52 – column 11, line 51), the operating system monitoring an application mix executing in the processor to determine a required frequency (note Fung '929: column 8, line 13 – column 11, line 16), and determining a minimum voltage at which the processor can operate at the required frequency (note Fung '463: [0035, 0056, 0069, 0070, 0072]), wherein the operating system directs the state machine to enter a state in which the required frequency is supplied by the clock signal generator (note Fung '929: column 16, lines 1-62) and a closest supported voltage equal to or greater than the minimum voltage is supplied by the voltage regulator (note Fung '463: [0035, 0056, 0069, 0070, 0072]), wherein the voltage regulator provides one of an idle voltage (note Fung '463: minimum CPU core voltage necessary to maintain CPU state info) or a peak voltage (note Fung '463: maximum rated voltage), wherein the voltage regulator can provide one voltage corresponding to each frequency supported by the clock signal generator (note Fung '463: [0035, 0056, 0069, 0070, 0072]).

Fung fails to disclose that the processor has a pad ring or that the processor core has an independent power supply.

AAPA discloses that a processor has a pad ring or that the processor core has an independent power supply (note page 1, line 20 – page 2, line 3).

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of a pad ring and processor core with an independent power supply, as AAPA teaches, in the system of Fung so as to allow for connection to external devices and enhance flexibility of the system by individually controlling power supplied to the core and pad ring.

b. As to claim 5, the claimed elements have already been discussed with respect to claim 4, with the exception of finding a minimum supported processor core voltage independently of a voltage required by a pad ring.

AAPA discloses providing separate power supplies for a processor core and pad ring (note page 1, line 20 – page 2, line 3).

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of a pad ring and processor core with an independent power supply, as AAPA teaches, in the system of Fung so as to allow for connection to external devices and enhance flexibility of the system by individually controlling power supplied to the core and pad ring.

c. As to claim 6, Fung discloses that a required frequency less than the maximum supported frequency is selected whenever a total processor core performance need of the current application mix can be met by a lower supported frequency (note Fung '463: [0056, 0070]).

d. As to claims 56-58, Fung discloses a method comprising determining a frequency for an application mix (note Fung '929: column 8, line 13 – column 11, line 16) and providing a voltage potential for the frequency (note Fung '463: [0035, 0056, 0069, 0070, 0072, 0151]), wherein providing a voltage potential includes providing a voltage potential to a core of a processor (note Fung '463: [0035, 0056, 0069, 0070, 0072, 0151]).

Fung fails to disclose that providing a voltage potential includes providing a different voltage potential to a pad of the processor.

AAPA discloses providing a different voltage potential to a processor core and pad ring (note page 1, line 20 – page 2, line 3).

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide different voltage potentials to a pad ring and processor core, as AAPA teaches, in the system of Fung so as to enhance flexibility of the system by individually controlling power supplied to the core and pad ring.

8. Claims 7-11 and 41-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fung 2002/0007463 A1, with Fung 5,710,929 incorporated by reference, in view of what was well known in the art at the time of the invention, as exemplified by McClure, 5,337,273.

a. As to claims 7-11, Fung discloses an apparatus comprising a RAM (note Fung '463: Figure 2, element 328), a processor coupled to the RAM (note Fung '463: Figure 2, element 320), a voltage regulator (note Fung '463: Figure 2, element 324) adapted to provide at least two voltage potential levels to at least a portion of the processor, and wherein the voltage potential level provided by the voltage regulator is adapted to be adjusted depending on a frequency corresponding to the operational load of the processor (note Fung '463: 0035, 0056, 0069, 0070, 0072]), wherein the voltage level is adapted to provide an idle voltage potential level (note Fung '463: minimum CPU core voltage necessary to maintain CPU state info) and a peak voltage level (note Fung '463: maximum rated voltage), further comprising a state machine (note Fung '929: state control unit 23 of column 6, lines 15-39) adapted to determine the operational

load of the processor, wherein the state machine is further adapted to determine a minimum voltage potential level at which the processor can operate (note Fung '929: state control unit 23 of column 6, lines 15-39), further comprising a clock signal generator (note Fung '463: Figure 2, element 342) adapted to provide a clock signal of at least two frequencies.

Fung fails to disclose that the RAM is an SRAM.

Examiner takes Official Notice that SRAMs are well known in the art for providing low power consumption and high access speed, as evidenced by McClure in column 1, lines 12-33.

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of SRAMs in the system of Fung, so as to further enhance the power conservation features of Fung by using a low power consumption SRAM memory.

b. As to claims 41-45, Fung discloses an article comprising a storage medium having stored instructions (note Fung '929: column 15, lines 35-39) thereon, that, when executed by a computing platform, results in monitoring an application mix executed by a processor (note Fung '929: column 8, line 13 – column 11, line 16), and adjusting the voltage potential level provided to at least a portion of the computing platform based on the application mix executed by the computing platform (note Fung '463: [0035, 0056, 0069, 0070, 0072, 0151]), wherein the instructions, when executed, further result in determining a preferred operational frequency based on the instruction mix executed by the computing platform (note Fung '929: column 15, line 35 – column 16, line 62), wherein the instructions, when executed, further result in computing platform executing the instruction mix at peak performance (note Fung '929: note Fung '929: column 8, line 13 – column 11, line 16 and column 15, line 35 – column 16, line 62), wherein the article further comprises an SRAM and the computing platform is coupled to the

SRAM, wherein the SRAM is adapted to store the instructions to be executed by the computing platform.

Fung fails to disclose an SRAM to store the instructions to be executed.

Examiner takes Official Notice that SRAMs are well known in the art for providing low power consumption and high access speed, as evidenced by McClure in column 1, lines 12-33.

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of SRAMs in the system of Fung, so as to further enhance the power conservation features of Fung by using a low power consumption SRAM memory.

9. Claims 46-48 and 53-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanikawa, 6,035,358 in view of Fung 2002/0007463 A1, with Fung 5,710,929 incorporated by reference.

a. As to claims 46-48, Tanikawa discloses a method comprising operating a core (note Figure 1, element 12) of a device at a voltage independent of a voltage that operates a pad ring (note Figure 1, element 13) of the device, further including operating the core at a voltage and operating the pad ring at a voltage different from the core, further including changing the voltage to the core without changing the voltage to pad ring (note column 1, lines 18-32 and column 3, lines 33-65).

Tanikawa fails to disclose that the core is operated at a minimum supported voltage.

Fung discloses operating a CPU core at a minimum supported voltage (note Fung '463: [0035, 0056, 0069, 0070, 0072, 0151]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to operate the CPU core at a minimum supported voltage, as Fung teaches, in the system of Tanikawa so as to provide for dynamic power conservation during the operation of the processor core.

b. As to claims 53-55, Tanikawa discloses a method comprising operating a processor core (note Figure 1, element 12) at a first voltage (note Figure 1, element 14) independent of a second voltage (note Figure 1, element 21) that operates a pad ring (note Figure 1, element 13) associated with the processor core, operating the pad ring at a voltage different from the processor core (note column 1, lines 18-32 and column 3, lines 33-65), changing the first voltage to the processor core without changing the second voltage to the pad ring (note column 3, lines 33-65).

Tanikawa fails to disclose that the first voltage is varied in accordance with changes in an operational load of the processor core.

Fung discloses that the first voltage is varied in accordance with changes in an operational load of the processor core (note Fung '463: [0035, 0056, 0069, 0070, 0072, 0151]), and operating the processor core at a minimum supported voltage (note Fung '463: [0035, 0056, 0069, 0070, 0072, 0151]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to vary the first voltage in accordance with changes in an operational load of the processor core and to operate the processor core at a minimum supported voltage, as Fung teaches, in the system of Tanikawa so as to provide for dynamic power conservation during the operation of the processor core.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, as the prior art teaches or suggests adjusting processor clock and/or voltage in response to changing operating parameters.

US Patents:	6,311,287	Dischler et al.	6,192,479	Ko
	5,825,674	Jackson	5,758,133	Evoy
	5,745,774	Munetsugu	5,745,375	Reinhardt et al.
	5,719,800	Mittal et al.	5,511,203	Wisor et al.
	5,475,847	Ikeda	5,218,704	Watts, Jr. et al.
	5,189,314	Georgiou et al.	5,142,684	Perry et al.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sumati Lefkowitz whose telephone number is 703-308-7790. The examiner can normally be reached on Monday-Friday from 6:00-2:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached at 703-305-4815.

The fax phone numbers for the organization where this application or proceeding is assigned are:

703-746-7238	for After-Final communications
703-872-9306	for Official communications
703-746-5661	for Non-Official/Draft communications

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Sumati Lefkowitz
Primary Examiner
Art Unit 2189

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November 12, 2003